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Chih-Yu (Andrew) Lai



Research Objective

Machine learning and quantitative modeling on time series, computer vision, and semiconductor manufacturing; design automation and hardware/software integration for bioelectronics.

Education	
Massachusetts Institute of Technology (MIT) - Cambridge, MA, USA	Jan 2022 – Present
Ph.D. in Electrical Engineering and Computer Science (GPA: 5.00/5.00)	
Selected Courses: Advances in Computer Vision, Inference and Information	
National Taiwan University (NTU) - Taipei, Taiwan	
M.S. in Bio-industrial Mechatronics Engineering (GPA: 3.94/4.00 - 35 credits)	Aug 2017 – Jul 2019
B.S. in Bio-industrial Mechatronics Engineering (<u>GPA: 3.68/4.00 - 188 credits</u>)	Aug 2013 – Jul 2017
Experiences	
 Research Intern, Applied Sciences Group, Microsoft Corporation Neural Text Image Compression [Ongoing] Introduced text logit loss that significantly reduces the character/word error rate supported by experimentation with state-of-the-art algorithms. 	Jun 2023 - Aug 2023 in text image compression,
PhD Researcher , Statistical Metrology Group (Prof. Duane Boning) <i>Physics-Informed Machine Learning for Semiconductor Manufacturing</i> [Ongoing]	Jan 2022 – Present
 Machine Learning on Time Series [NeurIPS-23] Proposed an algorithm for time series anomaly detection based on point/seq anomaly score which is proven superior under some conditions and outperforms 	uence. Derived an induced state-of-the-art models.
 Machine Learning in Computer Vision Realized speech-driven facial animation approach from noisy data using pre-trained 0 	GANs and seq2seq models.
Standard Cell Layout Designer , Taiwan Semiconductor Manufacturing Co. (TSMC) <i>Automated Placer, DLCAR, and PPA Estimator (AutoPDE)</i>	Dec 2019 – Jan 2022
• Developed an end-to-end automated system that can generate optimized standard ce placer, router, and machine learning based PPA estimator.	lls by integrating a transistor
• Invented DLCAR, a functional block-based standard cell routing system that c commercially manufacturable standard cell libraries within a few minutes for the N3	an generate functional and process node.
Design of Manufacturability in Advanced Technology Node	
 Pioneered in standard cell structure definition for the initial development stage of w being <u>first inventor of 8 US patents</u> for 3D IC and advanced structures. 	orld-class technology nodes,
Research Assistant, Academia Sinica	Aug 2019 – Nov 2019
• Served as research leader and secured research project grant (over 800,000NTD, Science and Technology for developing miniaturized bio-electronic platforms.	lyr project) from Ministry of
Graduate Researcher, Intelligent Bio-sensing Lab	Aug 2016 – Jul 2019
 Derived an <u>integral equation for modeling the diffusion impedance of interdigitated e</u> conformal mapping and the usage of Jacobi elliptic functions, elliptic integrals and Be is used for <u>modeling impedimetric tumor marker DNA biosensing data</u> obtained from unprecedentedly succeeded to extract underlying physical properties. 	<u>electrodes</u> (IDEs) by essel functions. The element n IDE chips and
Undergraduate Researcher, Lab of Computational Biology	Sep 2015 - Jul 2016
Big Data Analytics for Semiconductor Manufacturing	
 Implemented an ML stack method based on random forest and SVP models for predi- 	ction of key stages and tools

• Implemented an ML stack method based on random forest and SVR models for prediction of key stages and tools and won <u>1st prize</u> in the Big Data Analytics for Semiconductor Manufacturing contest held by TSMC.

Skills

- Languages: English (Fluent), Chinese Mandarin (Fluent), French (Elementary), Japanese (Elementary)
- Programming: C/C++, Python, MATLAB, SKILL, JavaScript, Visual Basic
- Tools: PyTorch, Tensorflow, Virtuoso, OpenCV, Solidworks, LabVIEW, COMSOL, Raspberry Pi

Publications

Conference Papers

- [1] <u>C.-Y. Lai</u> et al., <u>Nominality Score Conditioned Time Series Anomaly Detection by Point/Sequential Reconstruction</u>, *Neural Information Processing Systems (NeurIPS)*, 2023.
- [2] <u>C.-Y. Lai</u> et al., <u>Unsupervised Multivariate Time Series Anomaly Detection for High-Frequency Data</u>, *Microsystems Annual Research Conference (MARC)*, (2023).
- [3] <u>C.-Y. Lai</u> et al., MUC1 impedimetric aptasensing based on interdigitated array electrode chip using a novel diffusion element, *accepted to 31st Anniversary World Congress on Biosensors*, (2021).
- [4] <u>C.-Y. Lai</u> et al., <u>Diffusion impedance modeling for interdigitated array electrodes by conformal mapping and cylindrical finite length approximation</u>, *11th International Symposia on EIS*, (2019).
- [5] <u>C.-Y. Lai</u> et al., <u>Real-time impedimetric MUC1 aptasensor using microfluidic symmetric Au electrodes</u>, *The 22nd* International Conference on Miniaturized Systems for Chemistry and Life Sciences (µTAS), (2018).
- [6] <u>C.-Y. Lai</u> and L.-C. Chen, <u>EIS detection of MUC1 with two symmetric aptamer/Au electrodes</u>, 22nd Topical Meeting of the International Society of Electrochemistry, (2018).

Journal Papers

- [7] <u>C.-Y. Lai</u> et al., <u>Impedimetric aptasensing using a symmetric Randles circuit model</u>, *Electrochimica Acta* (IF = 6.216), **337** (2020) 35750.
- [8] <u>C.-Y. Lai</u> et al., <u>Diffusion impedance modeling for interdigitated array electrodes by conformal mapping and</u> <u>cylindrical finite length approximation</u>, *Electrochimica Acta*, **320** (2019) 134629.
- [9] J.-H. Weng, <u>C.-Y. Lai</u>, L.-C. Chen, <u>Microfluidic amperometry with two symmetric Au microelectrodes under one-</u> way and shuttle flow conditions, *Electrochimica Acta*, **297** (2019) 118-128.
- [10] M.-Y. Pan, D.-K. Yang, <u>C.-Y. Lai</u>, J.-H. Weng, K.-L. Lee, L.-C. Chen, C.-F. Chou, P.-K. Wei, <u>Spectral contrast imaging</u> <u>method for mapping transmission surface plasmon images in metallic nanostructures</u>, *Biosensors and Bioelectronics* (IF = 12.54), **142** (2019) 111545.

Selected Patents

- [11] <u>C.-Y. Lai</u> et al., <u>Integrated circuits having stacked transistors and backside power nodes</u>, *US Patent* App. 17/459,818, (2023).
- [12] <u>C.-Y. Lai</u> et al., <u>Semiconductor device having self-aligned interconnect structure and method of making</u>, *US Patent* App. 17/231,527, (2022).
- [13] C.-Y. Lai et al., Amphi-fet structure, method of making and method of designing, US Patent App. 17/214,194, (2022).

Honors and Awards

Golden Trade Secret Award, Trade Secret Competition – TSMC	2022
Golden Star Award, RD Idea Forum Competition - TSMC	2021
Best Presentation Award, DTP Conference - TSMC	2021
Golden Trade Secret Award, Trade Secret Competition – TSMC	2021
Best Presentation Award, DTP Conference - TSMC	2020
Honorable Mention, RD Idea Forum Competition – TSMC	2020
<u>1st Prize</u> , Big Data Analytics for Semiconductor Manufacturing – TSMC	2016
Presidential Award, National Taiwan University (Fall 2014)	2015
Entered Final Stage, Contestant Training Camp – Taiwan Olympiad in Informatics	2013

Selected Projects

Multi-Agent Reinforcement Learning (MARL) for "The Resistance"

May 2022

Jun 2018

• <u>Trained proximal policy optimization (PPO) agents to play the hidden role game The Resistance</u>, showing that emergent communication is helpful for cooperative and adversarial MARL for partially observable states.

Deep Q-Learning applied to Automated Forex Trading

• Developed a trading model for <u>profitable forex trading using a deep Q-network</u> that can automatically adapt to dynamic environments to maximize its profits. Constructed a <u>system for implementation of trading models</u>, automatic transaction, real-time price acquisition and forex history data storage using the LAMP software stack.